Remarks/Arguments

Claim Summary

By this Amendment, claims 1 and 15-19 have been revised, and new claim 20 has been added.

Claims 1-20 are now pending in the application.

35 U.S.C. §112, second paragraph

By this Amendment, claim 1 has been revised as suggested by the Examiner, and accordingly, Applicants respectfully request reconsideration of the rejection under 35 U.S.C. §112, second paragraph.

Allowable Subject Matter

Applicants acknowledge with thanks the indicated allowability of the subject matter defined by claims 1-14.

35 U.S.C. §103

Claims 15-19 were rejected under 35 U.S.C. §103 as being unpatentable over Ahmad et al. (US 5849615) in view of Yokozeki (US 6066894).

Without acquiescing to the reasoning underlying the rejection, independent claim 15 has been revised herein to more clearly define over the cited references.

In particular, claim 15 has been revised to recite the NMOS region of the semiconductor device being masked during the second implantation carried out in the PMOS region of the semiconductor device. (See, e.g., FIGS. 5B and 5C of the present application.) Also according to claim 15, after anneal/diffusion, the NMOS is formed having a single-LDD structure, while the PMOS is formed having a double-LDD structure. (See., e.g., FIGS. 10B and 10C of the present application.) The claimed method overcomes a drawback of conventional techniques in which the PMOS is particularly susceptible to short channel and hot carrier effects. (See, e.g., the last paragraph of page 17 of the present

specification.) In the meantime, the less-susceptible NMOS is formed with a single LDD structure, thus reducing the overall number of process steps.

Respectfully, Ahmad et al., taken alone or in combination with Yokozeki, does not teach or suggest the invention defined by claim 15.

That is, referring to FIG. 8 of Ahmad et al., this reference teaches the fabrication of a device in which the NMOS device (of region 16) is essentially a mirror image of the PMOS device (of region 13). Even if Ahmad et al. is modified in view of Yokozeki in the manner suggested by the Examiner, the resultant does not teach a configuration in which the NMOS device is formed with a single LDD structure and the PMOS device is formed with a double-LDD structure.

For at least the reasons stated above, Applicants contend that claims 15-20 would not have been obvious to one skilled in the art in view of the teachings of Ahmad et al. and Yokozeki.

Conclusion

No other issues remaining, reconsideration and early allowance of the present application are respectfully requested.

Respectfully submitted,

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Date: October 12, 2010